A 6 Watt LDMOS Broadband High Efficiency Distributed Power Amplifier Fabricated Using LTCC Technology

Lei Zhao, Anthony Pavio, Bob Stengel and Bruce Thompson

Solid State Research Center, ML-28, Motorola, Inc.
7700 S. River Parkway, Tempe, AZ 85284

Abstract — **A novel new approach in designing high efficiency power distributed amplifiers for broadband wireless applications has been developed. This synthesis technique allows the designer to achieve power added efficiencies, during class B operation, greater than 50% while still preserving the low VSWR and broadband characteristics of distributed structures. The performance of these newly designed amplifiers can yield the same PAE and power output performance of narrow band, single-ended, reactively matched amplifiers, without the high sensitivity to manufacturing variations. This synthesis technique has been applied to develop LDMOS and PHEMT distributed power amplifiers for cellular base stations and portable communication applications.**

I. Introduction

Distributed amplifiers and mixers have been used extensively for many years in a variety of broadband system applications such as microwave EW receivers, wide band transmitter exciters and low noise oscilloscope preamplifiers. However, these amplifiers have never demonstrated high efficiency and high power output performance. Distributed amplifier theory does not inherently limit power and efficiency performance obtainable, but proper control of device size, internal impedance and load impedance must be maintained [1-3]. This new synthesis method still relies on the use of artificial transmission line structures to form the amplifier's input and output networks, which absorb the parasitic capacitances of each active device in the chain; but, the new load targets vastly improve performance.

As with any distributed amplifier, multiple devices add power (more output current) to the output network and some additional gain to the amplifier. Since all of the distributed devices are imbedded within the same impedance conditions, power limiting occurs on the final device where the power accumulates at the output load. What this means is that all of the distortion or power limiting parameters are focused at only one of the devices in a conventional distributed amplifier implementation. Distributing the power limiting across all of the devices, while maintaining the benefit of broadband performance and conventional single-ended DC to RF power conversion efficiency would be the ideal goal for this new implementation of power amplifier.

II. Circuit Design

The bandwidth of a single-ended amplifier is limited by device and circuit parasitics. In addition, the ability to realize broadband high order matching networks is also difficult. An alternative approach to tuning out the parasitic reactances, associated with real devices, is to imbed these devices in artificial transmission line structures, yielding a frequency response beyond that of the discrete bandwidth optimized amplifier circuit.

Before continuing, it should be noted that the normal constraints used in designing power distributed amplifiers still apply, such as the phase shift per section of input and output line must be equal, as well as the drive signal at the input of each device must be equal. In addition, gate- and drain-line terminations must be provided for at least gain flatness reasons as well as for stability considerations. If we now consider the typical n-cell distributed amplifier shown in Figure 1, we first notice that one limitation to efficiency is the drain-line termination, which in a typical amplifier can lower the efficiency to about 25% (PAE). However, as we will see, the effects of this termination can be mitigated. Unlike an ideal transmission line, with characteristic impedance terminations, a distributed amplifier will have a virtual impedance as a result of the injected signals at each device output node. Figure 2 is a simple schematic of two ideal current sources combined at a common node connected to a load (R). Current through the load would be the sum of the two sources $i_1(t)$ and $i_2(t)$ where ω is the carrier frequency for both currents with independent phase values $\theta_1(t)$ and $\theta_2(t)$. Given these conditions, the next step will be to determine what impedance is seen by or loaded on the ideal sources. The impedance Z_1 looking into the common node with $i_2(t)$ in parallel with R is what current source vector $i_1(t)$ is loaded with and is equal to,

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$$Z_1 = v(t)/i_1(t) = R[i_1(t) + i_2(t)]/ i_1(t)$$
$$= R[1 + i_2(t) / i_1(t)] . \quad (1)$$

Replacing the current sources with their vector representation as a function of amplitude and phase, and

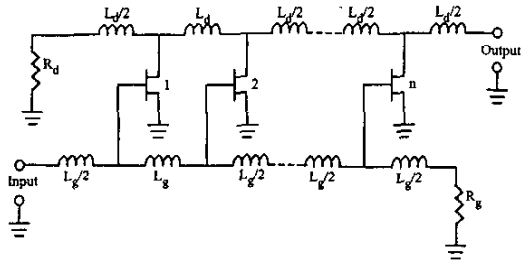

Figure 1 Classic distributed amplifier topology.

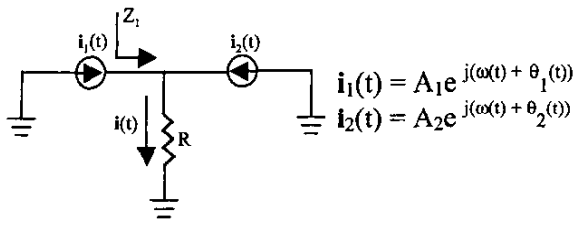

Figure 2 Current combining at a single node.

normalizing or setting ω equal to zero, the impedance Z_1 becomes,

$$Z_1 = R [1 + (A_2/ A_1)e^{j(\theta_2 - \theta_1)}] = R(1 + (A_2/ A_1)[\cos (\theta_2 - \theta_1) + j \sin (\theta_2 - \theta_1)]) . \quad (2)$$

However, if there is no phase offset or inphase combining is used, which is the expected condition in a distributed amplifier application, the amplitude of the reactive term becomes zero and the virtual impedance Z_1 is real only; hence,

$$Z_1 = R[1 + (A_2/ A_1)] \quad (3)$$

What this means is the values of the above equation would be integer multiples of R at each of the device output connection nodes. For the example shown in Figure 1, each of the current sources would be designed for a load impedance of R_L Ohms. Thus the output network of Figure 1, neglecting the termination, becomes the circuit shown in Figure 3. Here the objective was to operate each of the devices with identical conditions including the load impedance, (shown as R_L in Figure 3). Starting from the far right there are two currents summed into a common node with values i(t) from the device and 3*i(t) from the combined three devices to the left. Using the relation in Equation (3), the single device virtual impedance load is $[R_L/4](1+3/1)$, which is equal to R_L; while, the virtual load impedance seen by the next stage to the left is $R_L/3$. This is a crucial relationship, since it implies that the last section of transmission line must be designed with a characteristic impedance of $R_L/3$. Similarly, the next node to the left has a virtual impedance of R_L with a branch impedance to the left of $R_L/2$. By tapering the drain or output line characteristic impedance in this manner, the optimum load for either power output or efficiency, or a combination of the two impedances can be presented to each device.

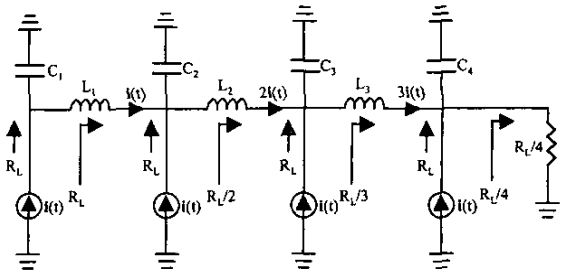

Figure 3 Current combining for a four-cell distributed

LTCC (low temperature co-fired ceramic) technology is an excellent choice for fabricating high power amplifiers by providing high density integration, low RF loss and good thermal dissipation. Discrete semiconductor devices can be placed directly on top of the thermal vias with diameter of 16 mil and filled with silver. These thermal vias provide good heat dissipation, which is very critical for a power amplifier. DuPont 951 ceramic tape is used in the designs reported in this paper.

III. PHEMT DISTRIBUTED PA DESIGN

Based on these concepts, a high efficiency, 2 Watt distributed amplifier for wireless applications was developed. A three-cell design, shown in Figure 4, was realized using LTCC technology circuit substrate and discrete PHEMT (1.9 mm) devices (Figure 5).

As with any power distributed amplifier, series gate capacitors were employed to equalize the RF drive signal on each gate, while series gate resistors were used to improve stability. In addition, the drain-line termination was set well above 50 ohms, since the impedance at that point in the circuit is approximately 150 Ohms. It should be noted that the drain termination could be made even larger at the expense of gain flatness and stability. However, only 1 or 2 percent of efficiency is lost due to

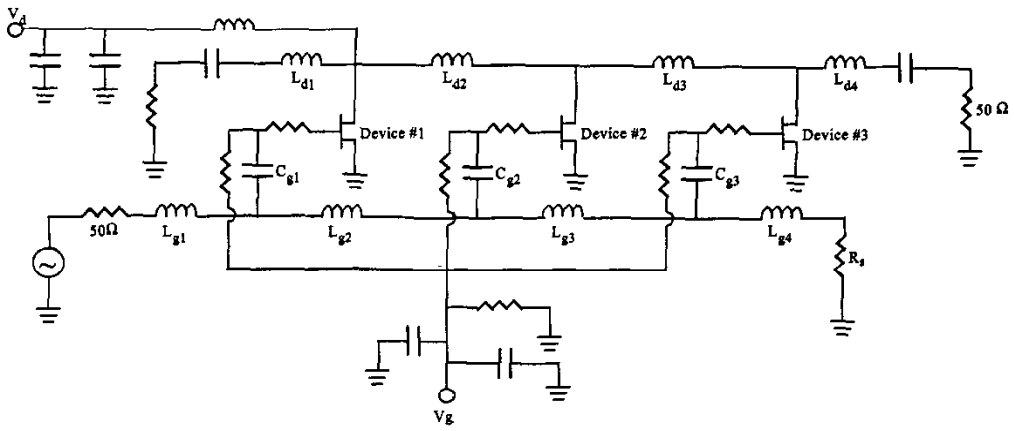

Figure 4 LTCC PHEMT distributed power amplifier schematic.

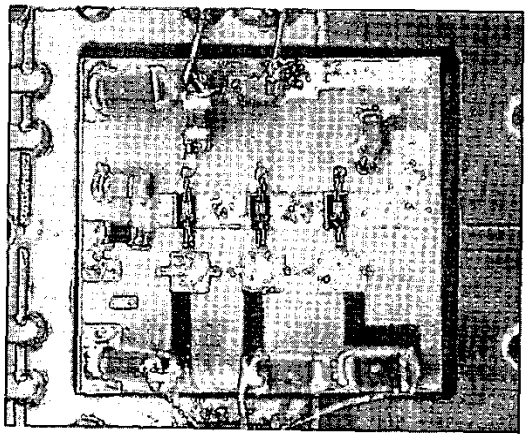

Figure 5 LTCC PHEMT distributed power amplifier.

this termination, due to the extensive drain-line impedance tapering employed in the amplifier. The small signal gain performance for the amplifier is shown in Figure 6.

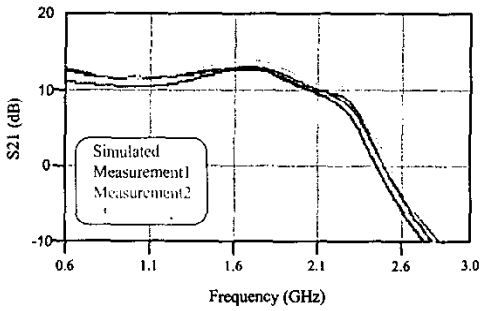

Figure 6 Amplifier small signal gain performance.

The amplifier used three 1.9 mm devices operated in class B with a 12 Vdc drain supply. The device size and supply voltage were chosen so that the amplifier output impedance would be 50 Ω and the output power level would be 2 Watts at saturation. The large signal performance of the amplifier is shown in Figure 7. As can be seen, the measured output power and efficiency performance is excellent. The dimension of the PA is 8.5 mm x 8 mm.

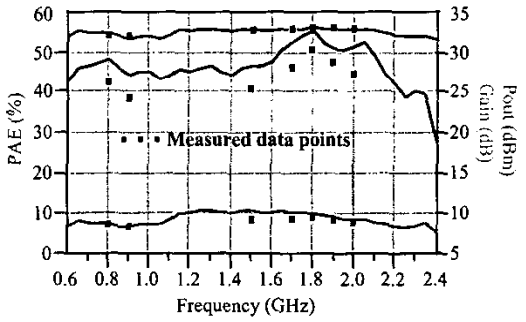

Figure 7 Amplifier large signal performance for 1.9 mm PHEMT device.

IV. LDMOS Distributed PA Design

A high efficiency, 6 Watt distributed amplifier, for wireless applications, was developed. The device size and the number of cells were chosen so that the amplifier's input and output impedances would be 50 Ω and the output power level would be 6 Watts at saturation. A five-cell design, shown in Figure 8, was realized using LTCC

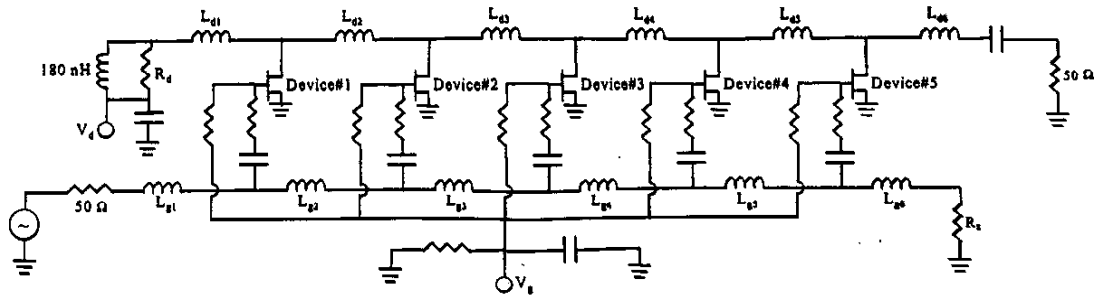

Figure 8 LTCC LDMOS distributed power amplifier schematic.

technology circuit substrate and discrete LDMOS (2.4 mm) devices (Figure 9). The PA is intended for use in the cellular base station applications as a driver amplifier covering from 100 MHz to 2 GHz with a DC supply of 28 Volts. The dimension of the PA is 10 mm x 9 mm.

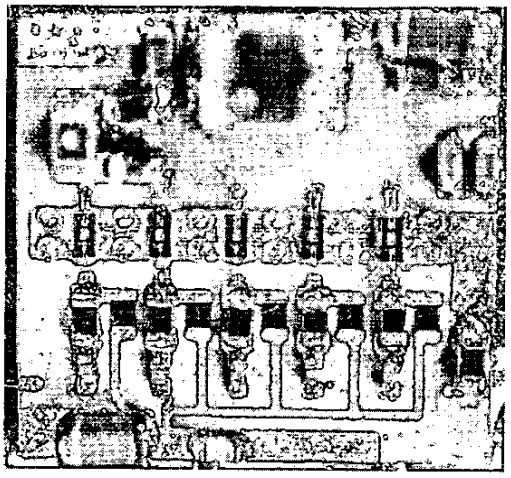

Figure 9 LDMOS distributed power amplifier.

The LTCC realization allows for the integration of most passive components, formation of thermal heat vias beneath the active devices, and for the realization of very low loss transmission lines. The use of thermal vias allows for a temperature rise of less than 5 °C between the active device and the heatsink. It should be noted that the loss in the drain-line structure is less than 0.5 dB at 2 GHz.

As with any distributed power amplifier, series gate capacitors were employed to equalize the RF drive signal on each gate, while employing series gate resistors to improve stability. A Coilcraft 1008HS 180 nH choke was used on the drain line to provide DC bias decoupling. The large signal performance of the amplifier is shown in Figure 10. As can be seen, the measured output power and efficiency performance is excellent.

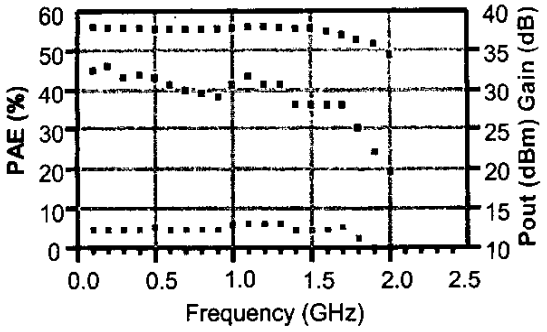

Figure 10 Amplifier large signal performance.

V. Conclusion

The above designs illustrate the dramatic improvement that can be obtained in power-added efficiency, when the drain transmission line is properly impedance tapered, and the devices are selected for the correct load impedance. The PAE performance presented here, for a distributed amplifier, is nearly twice as high as previously reported. It is also evident, from the above work, that broadband high efficiency amplifiers for wireless communications are clearly realizable. The circuit techniques presented in this paper have made possible a compact design that is suitable as a base station driver amplifier that covers from 100 MHz to 2 GHz with excellent efficiency. The above techniques can also be used to optimize the load impedance of a distributed amplifier for minimum distortion or maximum power output performance.

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